What is claimed is:

1. A PHY responsive to first and second voltages on a network medium, the PHY comprising:

a capacitor;

a first current source to charge the capacitor by conducting a first conduction current indicative of the magnitude of the difference of the first and second voltages; and

a transistor to discharge the capacitor for a discharge time interval by conducting a transistor conduction current, the transistor coupled to the capacitor so that the transistor conduction current decreases in magnitude as the capacitor discharges during the discharge time interval.

2. The PHY as set forth in claim 1, the capacitor having a voltage difference, wherein the transistor is a pullup pMOSFET having a gate voltage responsive to the capacitor voltage difference.

3. The PHY as set forth in claim 1, the capacitor having a voltage difference, wherein the transistor is a pulldown nMOSFET having a gate voltage responsive to the capacitor voltage difference.

4. The PHY as set forth in claim 1, further comprising:

a second current source to charge the capacitor by conducting a second conduction current, wherein the second conduction current source is coupled to the

transistor so that the fraction of the second conduction current used to charge the capacitor increases as the transistor conduction current decreases.

5. The PHY as set forth in claim 4, wherein the second current source comprises:

a differential pair of transistors; and

a current source transistor cascaded with the differential pair of transistors.

6. The PHY as set forth in claim 1, further comprising:

a second current source to charge the capacitor by conducting a second conduction current, wherein the second current source charges the capacitor only if the transistor is ON.

7. The PHY as set forth in claim 4, further comprising:

a second current source to charge the capacitor by conducting a second conduction current, wherein the second current source charges the capacitor only if the transistor is ON.

8. The PHY as set forth in claim 4, wherein the second conduction current is indicative of the magnitude of the difference of the first and second voltages.

9. An envelope detector to detect the envelope of a differential voltage signal, the envelope detector comprising:

a node;

a capacitor connected to the node, the node having a node voltage;

a first current source to charge the capacitor so that the node voltage is indicative of the magnitude of the differential voltage signal;

a transistor having a gate connected to the node;

a second current source coupled to the node; and

an output buffer coupled to the node to provide an output voltage indicative of the node voltage;

wherein if the output voltage crosses a threshold, the transistor and the second current source in combination are coupled to the node to discharge the capacitor.

10. The envelope detector as set forth in claim 9, wherein the second current source comprises:

a differential pair of transistors; and

a current source transistor cascaded with the differential pair of transistors.

11. The envelope detector as set forth in claim 9, wherein

the first current source is connected to the node to sink a first current from the node indicative of the magnitude of the differential voltage signal;

the transistor is a pMOSFET; and

the transistor and the second current source in combination are coupled to the node to source a second current to the node if the output voltage crosses the threshold.

12. The envelope detector as set forth in claim 11, wherein

the pMOSFET has a drain current;

the second current source conducts a conduction current; and

the magnitude of the drain current is equal to the sum of the magnitude of the second current and the magnitude of the conduction current.

13. The envelope detector as set forth in claim 12, wherein

the conduction current source is indicative of the magnitude of the differential voltage signal.

14. The envelope detector as set forth in claim 9, wherein

the first current source is connected to the node to source a first current to the node indicative of the magnitude of the differential voltage signal;

the transistor is a nMOSFET; and

the transistor and the second current source in combination are coupled to the node to sink a second current from the node if the output voltage crosses the threshold.

15. The envelope detector as set forth in claim 14, wherein

the nMOSFET has a drain current;

the second current source conducts a conduction current; and

the magnitude of the drain current is equal to the sum of the magnitude of the second current and the magnitude of the conduction current.

16. The envelope detector as set forth in claim 15, wherein

the conduction current source is indicative of the magnitude of the differential voltage signal.

17. A communication system comprising:

a network medium comprising home phone wiring; and

a PHY responsive to first and second voltages on the home phone wiring, the PHY comprising:

a node having a node voltage;

a buffer to provide an output voltage indicative of the node voltage;

a capacitor connected to the node;

a first current source to charge the capacitor by conducting a first conduction current indicative of the magnitude of the difference of the first and second voltages; and

a FET to discharge the capacitor for a discharge time interval by conducting a drain current, the FET having a gate voltage responsive to the node voltage.

18. The communication system as set forth in claim 17, further comprising:

a MAC, wherein the PHY provides to the MAC an indication of detection if the output voltage crosses a threshold.

19. The communication system as set forth in claim 18, further comprising:

a second current source coupled to the node, wherein the FET and the second current source in combination discharge the capacitor during the discharge time interval.

20. A method to communicate via home phone wiring, the method comprising:

propagating information on the home phone wiring using pulse position modulation;

charging a capacitor with a current indicative of the full-wave rectification of a received differential voltage signal on the home phone wiring, the capacitor having a charge voltage;

buffering the capacitor charge voltage to provide an output voltage; and

discharging the capacitor if the output voltage crosses a threshold by conducting drain current through a FET , wherein the FET has a gate voltage responsive to the capacitor charge voltage.